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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,788	01/15/2004	Thomas Michael Gooding	ROC920030335US1	5462

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EXAMINER	
THORNEWELL, KIMBERLY A	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,788	GOODING ET AL.	
	Examiner	Art Unit	
	Kimberly Thornewell	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 were originally presented for examination. In the Office Action dated 5/19/2006, all claims were rejected. In the response dated 8/8/2006, the Applicant amended claims 3 and 13, and therefore all of claims 1-16 remain pending in the instant application.

Response to Arguments

2. *Response: Claim Objections*

The Examiner thanks the Applicant for amending claim 3 in order to correct its dependency. Accordingly, the objection to claim 3 for informalities is withdrawn.

3. *Response: Section 101 Rejections*

Because claim 13 is now limited to tangible embodiments of the computer-readable medium, the rejection of claims 13-16 under Section 101 is withdrawn.

4. *Response: Section 103 Rejections*

Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 9, 10, 12-14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu, "Fault Tolerance in Adaptive Real-Time Computing Systems," a doctoral dissertation for Stanford University dated December 2001.

As per claim 9,

Yu discloses a method for the automatic reconfiguration of faulty signal wires in a logic simulation hardware emulator, the logic simulation hardware emulator having one or more source emulation processors coupled to one or more receiving emulation processors by a set of emulation cables, each emulation cable having a plurality of signal wires; the plurality of signal wires comprising a plurality of regular signal wires and one or more predefined spare signal wires (**page 60 figure 6-6**, *source processor FPGA1, receiving processor FPGA2, containing two regular wires and one spare wire, cable is implied as it is only used to bound the wires together*), the method comprising the steps of:

- Identifying a set of faulty signal wires within the plurality of regular signal wires, if any faulty signal wires exist (**page 60 last paragraph,** *fault location*); and
- Reassigning signals from the set of faulty signal wires to one or more spare signal wires within the set of emulation cables (**page 60 figure 6-6 b and c**).

As per claim 10,

Yu discloses performing a connectivity diagnostic on the emulation cable within the hardware emulator (**page 61 first full paragraph**, *location of interconnect fault*).

As per claim 12,

Yu discloses the step of reassigning signals from the set of faulty signal wires to one or more spare signal wires within the set of emulation cables including the steps of:

- Determining if a spare signal wire is available, if one or more faulty signal wires exist (**page 60 first paragraph**);
- Setting a source module spare register to a value corresponding to the source emulation processor having the faulty wire (**page 62 table 6-2**); and
- Changing any receiving emulation processor steps sourced by the faulty wire to the spare wire (**page 60 figure 6-6b, also page 62 first full paragraph**).

As per claim13,

Yu discloses a computer-readable program stored on a tangible computer-readable medium, the computer readable program providing the automatic reconfiguration of faulty signal wires in a logic simulation hardware emulator, the logic simulation hardware emulator having one or more source emulation processors coupled to one or more receiving emulation processors by a set of emulation cables, each emulation cable having a plurality of signal wires; the plurality of signal wires comprising a plurality of regular signal wires and one or more predefined spare signal wires (**page 60 figure 6-6**, *source processor FPGA1, receiving processor FPGA2, containing two regular wires and one spare wire, cable is implied as it is only used to bound the wires together*), the method comprising the steps of:

- Identifying a set of faulty signal wires within the plurality of regular signal wires, if any faulty signal wires exist (**page 60 last paragraph,** *fault location*); and
- Reassigning signals from the set of faulty signal wires to one or more spare signal wires within the set of emulation cables (**page 60 figure 6-6 b and c**).

As per claim 14,

Yu discloses performing a connectivity diagnostic on the emulation cable within the hardware emulator (**page 61 first full paragraph**, *location of interconnect fault*).

As per claim 16,

Yu discloses the step of reassigning signals from the set of faulty signal wires to one or more spare signal wires within the set of emulation cables including the steps of:

- Determining if a spare signal wire is available, if one or more faulty signal wires exist (**page 60 first paragraph**);
- Setting a source module spare register to a value corresponding to the source emulation processor having the faulty wire (**page 62 table 6-2**); and

Changing any receiving emulation processor steps sourced by the faulty wire to the spare wire (**page 60 figure 6-6b, also page 62 first full paragraph**).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-6, 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, "Fault Tolerance in Adaptive Real-Time Computing Systems," a doctoral dissertation for Stanford University dated December 2001, in view of Babb et al., "Logic Emulation with Virtual Wires," published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No.6, June 1997.

As per claim 1,

Yu teaches a logic simulation hardware emulator, comprising:

- One or more source emulation processors (**page 60 figure 6-6,** *FPGA1*) coupled to one or more receiving emulation processors (**page 60 figure 6-6**, *FPGA2*) by an emulation cable having a plurality of signal wires (**page 60 figure 6-6**, *3 wires; the cable is implied, since it is only meant to bound the connecting wires together*), the plurality of signal wires comprising a plurality of regular signal wires (**page 60 figure 6-6**, *solid wires*) and one or more spare signal wires (**page 60 figure 6-6**, *dashed wire*); and
- A runtime control program for controlling the emulation processors (**page 58 figure 6-5, also bottom paragraph on page 58**), wherein upon detection of a fault on a regular signal wire, the runtime control program reassigns a signal on

the regular signal wire having the fault to one or more spare signal wires (**page 60 figure 6-6** *shows signal reassignment*; **page 61 figures 6-7 and 6-8** *show reconfiguration, also* **page 61 first full paragraph**).

Although Yu discloses simulated square wave responses for systems on page 88-89 and Table 1, which implies that simulation is performed on the interconnected emulation processors, Yu does not disclose expressly the emulation processors being embodied in a simulation model, or the runtime control program controlling the simulation model. However, the emulation processors as disclosed in Yu are actually FPGAs. Babb discloses the simulation of interconnected FPGA chips based on a simulation model (**page 616 section III first paragraph,** *"virtualization"*), and using a runtime control program for controlling the simulation model (**page 616 figure 16**) and for configuring the wires interconnecting FPGA chips (**page 615 figure 12**).

It would have been obvious to one of ordinary skill in the art of emulation of simulation hardware, at the time of the present invention, to modify Yu's spare wire rerouting system of emulation processors with Babb's method of simulating interconnected FPGA chips in order to simulate fault detection and recovery in wires connecting the emulation processors. The motivation for doing so would have been to exploit predictability of the processors by running them on a simulation processor, ultimately improving bandwidth in connections between chips (**Babb page 610 column 2 last paragraph**).

As per claim 2,

Babb discloses the signal wires being defined at simulation model build time (**page 614 figure 11**). Combined with the teachings of Yu as applied to claim 1 above, it would have been obvious for Babb to define all wires, including the spare signal wires at simulation model build time.

As per claim 3,

Yu discloses the spare signal wires being defined when one or more of the emulation processors and their corresponding regular signal wires is found faulty (**page 60 first paragraph lines 7-13**). Babb discloses configuring the emulation processors and their corresponding wires at simulation model build (**page 614 figure 11**). It would have been obvious to modify Yu's fault detection with Babb's processor simulation in order to designate the processors and their corresponding wires as faulty at simulation model build. The motivation for doing so would have been to improve predictability (**Babb page 610 column 2 last paragraph**).

As per claim 4,

Yu discloses FPGA repairing faults by selecting (multiplexing) configurations that avoid the fault (**page 51 last paragraph – page 52 lines 1-4**). Yu further discloses avoiding faults by reconfiguring routes between processors with spare wires (**page 60 figure 6-6**). Babb discloses the logic simulation hardware emulator comprising a wire select multiplexer, the inputs of the wire select multiplexer coupled to the outputs of the one or more source emulation processors, and the output of the wire select multiplexer coupled to the input of the emulation cable (**page 1 column 2 second full paragraph**).

As per claim 5,

Yu discloses the spare signal selection being provided by a spare select register (**page 61 last paragraph**).

As per claim 6,

Yu discloses the spare select register being updated by the runtime control program (**page 62 first full paragraph**, *coding of the faulty wire identification*).

As per claim 11,

Although Yu discloses simulated square wave responses for systems on page 88-89 and Table 1, which implies that simulation is performed on the interconnected emulation processors, Yu does not disclose expressly predefining one or more spare signal wires within the emulation cable at simulation model build time. Babb discloses the simulation of interconnected FPGA chips based on a simulation model (**page 616 section III first paragraph**, *"virtualization"*), and the signal wires being defined at simulation model build time (**page 614 figure 11**).

It would have been obvious to one of ordinary skill in the art of simulation of emulation of simulation hardware, at the time of the present invention, to modify Yu's use of spare wires with Babb's method of simulating interconnected FPGA chips in order to simulate fault detection and recovery in wires connecting the emulation processors. The motivation for doing so would have been to exploit predictability of the processors by running them on a simulation

processor, ultimately improving bandwidth in connections between chips (**Babb page 610 column 2 last paragraph**).

As per claim 15,

Although Yu discloses simulated square wave responses for systems on page 88-89 and Table 1, which implies that simulation is performed on the interconnected emulation processors, Yu does not disclose expressly predefining one or more spare signal wires within the emulation cable at simulation model build time. Babb discloses the simulation of interconnected FPGA chips based on a simulation model (**page 616 section III first paragraph**, *"virtualization"*), and the signal wires being defined at simulation model build time (**page 614 figure 11**).

It would have been obvious to one of ordinary skill in the art of simulation of emulation of simulation hardware, at the time of the present invention, to modify Yu's use of spare wires with Babb's method of simulating interconnected FPGA chips in order to simulate fault detection and recovery in wires connecting the emulation processors. The motivation for doing so would have been to exploit predictability of the processors by running them on a simulation processor, ultimately improving bandwidth in connections between chips (**Babb page 610 column 2 last paragraph**).

9. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Babb as applied to claims 1-6 above, and further in view of Rush, US Patent no. 5,742,181.

As per claim 7,

Babb discloses the simulation hardware emulator comprising source type multiplexers coupled to an output of the emulation cable and having a select signal (**page 617 column 1 lines 9-11**). Babb does not disclose expressly a plurality of processor selector multiplexers coupled to the one or more source type multiplexers. Rush discloses an FPGA interconnect architecture designed for hardware emulation (**column 1 lines 23-26**) that incorporates a plurality of multiplexers for FPGA (emulation processor) selection, coupled to an input of receiving emulation processors (**column 10 lines 15-26**), each processor selector multiplexer having a select signal (**column 9 line 63-column 10 line 1**).

It would have been obvious for one of ordinary skill in the art of emulation of simulation hardware, at the time of the present invention to modify Yu's spare wire rerouting system of emulation processors with Babb's method of simulating interconnected FPGA chips in order to simulate fault detection and recovery in wires connecting the emulation processors. It also would have been obvious to further modify Yu/Babb's system of spare wire rerouting simulation with Rush's multiplexer architecture for interconnected FPGA's in order to provide a select signal for each of the emulation processors for the simulation hardware emulator. The motivation for doing so would have been to enable selective switching between adjacent emulation processors (**Rush column 10 lines 25-33**).

As per claim 8,

Babb discloses select signals from multiplexers being provided by the runtime control program (**page 617 column 1 second full paragraph**). Combined with Yu and Rush as applied

to claim 7 above, it would have been obvious to provide the select signals for both the source type multiplexer and the processor selector multiplexer by the runtime control program.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment," by Tessier et al., published for the MIT Laboratory for Computer Science, October 2001.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly Thornewell whose telephone number is (571)272-6543. The examiner can normally be reached on 8am-4:30pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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